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**1 110-GB/s simultaneous bidirectional transceiver logic synchronized with a system clock**

Takahashi, T.; Muto, T.; Shirai, Y.; Shirotori, F.; Takada, Y.; Yamagiwa, A.; Nishida, A.; Hotta, A.; Kiyuna, T.;  
 Solid-State Circuits, IEEE Journal of, Volume: 34, Issue: 11, Nov. 1999  
 Pages:1526 - 1533

[\[Abstract\]](#) [\[PDF Full-Text \(552 KB\)\]](#) **IEEE JNL**

**2 A 250-Mb/s/pin, 1-Gb double-data-rate SDRAM with a bidirectional delay and an interbank shared redundancy scheme**

Takai, Y.; Fujita, M.; Nagata, K.; Isa, S.; Nakazawa, S.; Hirobe, A.; Ohkubo, H.; Sakao, M.; Horiba, S.; Fukase, T.; Takaishi, Y.; Matsuo, M.; Komuro, M.; Uchida, T.; Sakoh, T.; Saino, K.; Uchiyama, S.; Takada, Y.; Sekine, J.; Nakanishi, N.; Oikawa, T.; Igeta, M.; Tanabe, H.; Miyamoto, H.; Hashimoto, T.; Yamaguchi, H.; Koyama, K.; Kobayashi, Y.; Okuda, T.;  
 Solid-State Circuits, IEEE Journal of, Volume: 35, Issue: 2, Feb. 2000  
 Pages:149 - 162

[\[Abstract\]](#) [\[PDF Full-Text \(340 KB\)\]](#) **IEEE JNL**

**3 Hybirdly integrated optical transceiver module for access networks**

Uno, T.; Nishikawa, T.; Mitsuda, M.; Tohmon, G.; Matsui, Y.;  
 Electronic Components and Technology Conference, 1998. 48th IEEE, 25-28 May 1998  
 Pages:560 - 565

[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) **IEEE CNF**

**4 Built-in parametric test for controlled impedance I/Os**

Haulin, T.;  
 VLSI Test Symposium, 1997., 15th IEEE, 27 April-1 May 1997  
 Pages:123 - 128

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[\[Abstract\]](#) [\[PDF Full-Text \(480 KB\)\]](#) [IEEE CNF](#)

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**5 A c m pact array pr cessor based n self-timed simultane us  
bidirecti nal signalling**

*Yacoub, G.Y.; Soni, T.; Ku, W.H.;*

Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium  
on , 3-6 May 1993

Pages:1893 - 1896 vol.3

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[\[Abstract\]](#) [\[PDF Full-Text \(336 KB\)\]](#) [IEEE CNF](#)

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**6 Simultaneous bidirectional signalling for IC systems**

*Lam, K.; Dennison, L.R.; Dally, W.J.;*

Computer Design: VLSI in Computers and Processors, 1990. ICCD '90.

Proceedings., 1990 IEEE International Conference on , 17-19 Sept. 1990

Pages:430 - 433

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[\[Abstract\]](#) [\[PDF Full-Text \(404 KB\)\]](#) [IEEE CNF](#)

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**7 Signal integrity analysis of high-speed, high-pin-count digital packages**

*Tsai, C.-T.;*

Electronic Components and Technology Conference, 1990. Proceedings., 40th , 20-  
23 May 1990

Pages:1098 - 1107 vol.2

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**1 A massively parallel reverse modeling approach for semiconductor devices and circuits**

*Wu, S.; Vai, M.;*

High Speed Semiconductor Devices and Circuits, 1997. Proceedings., 1997

IEEE/Cornell Conference on Advanced Concepts in , 4-6 Aug. 1997

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**2 Control and implementation of a three-phase voltage-doubler reversible AC to DC converter**

*Ching-Tsai Pan; Maoh-Chin Jiang;*

Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual

IEEE , Volume: 1 , 18-22 June 1995

Pages:437 - 443 vol.1

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**3 Signal integrity analysis of high-speed, high-pin-count digital packages**

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Electronic Components and Technology Conference, 1990. Proceedings., 40th , 20-23 May 1990

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Pages:437 - 443 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(456 KB\)\]](#) **IEEE CNF**

**2 Analysis of distributed erbium-doped fiber amplifiers with fiber background loss**

*Desurvire, E.;*

Photonics Technology Letters, IEEE , Volume: 3 , Issue: 7 , July 1991

Pages:625 - 628

[\[Abstract\]](#) [\[PDF Full-Text \(292 KB\)\]](#) **IEEE JNL**

**3 A new double modeling approach for dynamic cardiac PET studies using noise and spillover contaminated LV measurements**

*Dagan Feng; Xianjin Li; Sung-Cheng Huang;*

Biomedical Engineering, IEEE Transactions on , Volume: 43 , Issue: 3 , March 1996

Pages:319 - 327

[\[Abstract\]](#) [\[PDF Full-Text \(888 KB\)\]](#) **IEEE JNL**

**4 A massively parallel reverse modeling approach for semiconductor devices and circuits**

*Wu, S.; Vai, M.;*

High Speed Semiconductor Devices and Circuits, 1997. Proceedings., 1997

IEEE/Cornell Conference on Advanced Concepts in , 4-6 Aug. 1997

Pages:201 - 209

[\[Abstract\]](#) [\[PDF Full-Text \(496 KB\)\]](#) **IEEE CNF**

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**5 Modular-additive signature analysis for built-in self-test**

*Cheng-Wen Wu; Hun-Song Chen;*

European Test Conference, 1993. Proceedings of ETC 93., Third, 19-22 April 1993

Pages:457 - 465

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[\[Abstract\]](#) [\[PDF Full-Text \(676 KB\)\]](#) [IEEE CNF](#)

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**6 Signal integrity analysis of high-speed, high-pin-count digital packages**

*Tsai, C.-T.;*

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Pages:1098 - 1107 vol.2

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**1 Enhancement of the cooling performance of circular pin fin heat sinks under flow bypass conditions**

*Jonsson, H.; Moshfegh, B.;*

Thermal and Thermomechanical Phenomena in Electronic Systems, 2002. ITERM 2002. The Eighth Intersociety Conference on, 30 May-1 June 2002  
Pages:425 - 432

[\[Abstract\]](#) [\[PDF Full-Text \(756 KB\)\]](#) **IEEE CNF**

**2 Local convection heat transfer coefficient measurement in a wavy channel with flow disturbers**

*Dini, S.; Veronesi, R.R.; Huff, R.K.;*

Thermal and Thermomechanical Phenomena in Electronic Systems, 2002. ITERM 2002. The Eighth Intersociety Conference on, 30 May-1 June 2002  
Pages:718 - 725

[\[Abstract\]](#) [\[PDF Full-Text \(861 KB\)\]](#) **IEEE CNF**

**3 Multi-dimensional cluster analysis of class characteristics for ballistics specimen identification**

*Smith, C.L.;*

Security Technology, 2001 IEEE 35th International Carnahan Conference on, 16-19 Oct. 2001  
Pages:115 - 121

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**1 Thermal Studies on Pin Grid Array Packages for High Density LSI and VLSI Logic Circuits**

*Mahalingam, L.; Andrews, J.; Drye, J.;*

Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [see also IEEE Trans. on Components, Packaging, and Manufacturing Technology, Part A, B, C] , Volume: 6 , Issue: 3 , Sep 1983

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[\[Abstract\]](#) [\[PDF Full-Text \(1504 KB\)\]](#) **IEEE JNL**

**2 Multi-dimensional cluster analysis of class characteristics for ballistics specimen identification**

*Smith, C.L.;*

Security Technology, 2001 IEEE 35th International Carnahan Conference on , 16-19 Oct. 2001

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